REMARKS

Claims 1-17 are presented for further examination. Claims 1-14 have been amended.

In the Office Action mailed September 25, 2003, the Examiner objected to the disclosure because of informalities at page 4, line 9; page 5, lines 8-15; and page 6, line 4. Applicant has amended the specification as noted by the Examiner to overcome the informalities.

Claims 1, 5, and 14 were objected to because the acronym (TAP) should be inserted after the first occurrence of "test access port." Claims 1-17 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,054,024 ("Whetsel").

In the remarks accompanying the rejection, the Examiner states that the Whetsel reference discloses in Figure 5 the elements CBXa, CBXb, and number 74 at Figure 2, "selectively driving the TAP functions of the plurality of components with respective clocks." The remarks further state that with respect to claims 2, 6, 10, 11, and 15, that generating respective clocks for the TAP functions is disclosed in Whetsel at Figure 2, number 74, and that in claims 4, 8, 13, and 17 the operation "of generating respective clocks on board a single chip" is disclosed in Whetsel at Figure 2, number 74.

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

In the disclosed and claimed embodiments of the invention, a process for management of a test access port (TAP) function is provided wherein each component on a single chip is provided with a respective TAP function. Each TAP function is driven by a dedicated clock signal generated by a dedicated clock signal generator (*e.g.*, *see* page 5, line 2 and Figure 2). Each of the dedicated clock signals are transmitted to their respective TAP function by a shared bus line while at least one further signal, such as test data input (TDI), test data output (TDO), test mode select (TMS) is provided on a separate line.

In Whetsel, U.S. Patent No. 5,054,024, a system scan path architecture with remote bus controller is provided. Whetsel discloses in Figure 1 a primary bus master (12) transmitting a test clock signal (TCK) to a plurality of device select modules (DSM 18a, 18b). As shown in the circuit diagram of a representative device select module 18 in Figure 4, the test

clock signal TCK is received at a buffered input 24 and passes directly to a buffered output 52 as a device test clock signal (DTCK).

The device referenced by the Examiner in Figure 2, reference number 74, is the test mode select selection circuit (TMS SEL CKT) that receives as input a test mode select signal (TMS) and an optional test mode select input (OTMS) (*see* column 6, line 62) and outputs via buffers 44 device test mode select signals 1-4 (DTMS1-DTMS4) (*see* Whetsel column 6, lines 24-64).

The Examiner asserts that Figure 5 shows the use of a plurality of clock signals CBXaCBXb. However, applicant cannot find any such reference in Figure 5 of Whetsel. Rather, the example implementation of a test mode select circuit (TMS SEL CKT) is shown in Figure 4 in which a plurality of control bit inputs (CBxA and CBxB) are illustrated and described at column 9, lines 43-46. As shown in Figure 4, these signals comprise control bit pairs that are input to each multiplexer 100-106 via respective AND gates. Nowhere does Whetsel teach or suggest that these are clock signals. Thus, Whetsel does not teach or suggest the use of dedicated clock signals generated by dedicated clock signal generators in connection with a shared bus line for driving individual TAP functions on a single chip.

Turning to the claims, claim 1 is directed to a process for management of a test access port (TAP) function in a plurality of components arranged on a single chip, each of the components provided with a respective TAP function adapted to be driven by a respective dedicated clock and by at least one further signal that includes the operations of using the at least one further signal in a shared way between the TAP functions and a plurality of components and selectively driving the TAP functions of the plurality of components with the respective dedicated clocks. As discussed above, Whetsel teaches the use of only a single clock signal, TCK. The TMS SEL CKT 74 in Figure 2 is a test mode select selection circuit that outputs device test mode selection signals 1-4 in response to test mode select and optional test mode select signals received via input buffers 24, 82 respectively. The signals CBxA and CBxB are control bit inputs for the test mode select circuit 74. Hence, Whetsel does not teach or suggest the combination recited in claim 1.

Dependent claims 2-4 all recite the use of dedicated clocks and would be allowable for the reasons discussed above with respect to claim 1. Independent claims 5, 9, and 14 all recite the use of dedicated clocks for each individual tap function associated with a respective plurality of components arranged on a single chip. Applicant submits these claims are allowable for the reasons discussed above with respect to claim 1 in that Whetsel does not teach or suggest the use of separate dedicated clock signals for driving separate TAP functions.

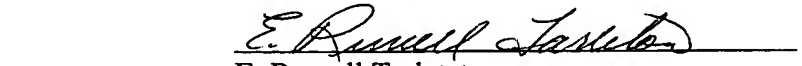
Dependent from these claims are further dependent claims that are directed to additional features of the invention, including separate dedicated clock signal generators and respective separate dedicated clock signal pull-down functions. Whetsel does not teach or suggest either of these functions in combination with the elements recited in the associated independent claims.

In view of the foregoing, applicant submits that all of the claims in this application are clearly in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



E. Russell Tarleton
Registration No. 31,800

ERT:aep/gc

Enclosure:
Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

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